MATERIALS FOR ADVANCED PACKAGING IN MICROELECTRONICS - MATERIALS SCIENCE AND ENGINEERING, PRODUCT PERFORMANCE AND RELIABILITY

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The goal of the lecture is to provide knowledge about thin film materials used in silicon-based semiconductor industry and to explain the role of advanced materials for functionality, performance and reliability of microelectronic products as well as their process integration. Material transitions that are necessary to improve the product performance and to maintain the product reliability are highlighted. The interdisciplinary character of materials research and development for semiconductor industry is demonstrated based on typical examples. The close interaction between design, technology and materials is shown. In particular, it will be demonstrated how new design and technology approaches as well as new materials provide the pathway to new products with more functionality and higher performance. Analytical techniques for multi-scale materials characterization in µm and nm ranges are covered as well. The role of the materials scientist and engineer in research and technology development in semiconductor industry is explained.

The focus of this lecture will be primarily on challenges for advanced packaging based-on three-dimensional (3D) Through Silicon Via (TSV) IC integration, a technology approach that creates highly integrated systems by vertical stacking and by connecting various processes, materials and functional components. The potential benefits of 3D IC integration will vary depending on the chosen approach and the application. They include increased performance, reduced power and small form factor as well as multifunctionality and flexible heterogeneous integration. Managing materials compatibility and internal mechanical stress is a key task to ensure high performance and high reliability of products manufactured in advanced nodes of CMOS-based semiconductor technology. The role of materials science and engineering for the deployment of new technologies for advanced packaging of ICs like 3D TSV integration will be demonstrated.

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